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Design and characterization of a CMOS compatible poly-SiGe low-g capacitive accelerometer

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Abstract

This paper presents the design and characterization of a CMOS compatible low-g capacitive accelerometer, fabricated in a low thermal budget poly-SiGe MEMS technology. The out-of-plane single axial device features a large effective capacitive surface, low cross talk and a robust beam suspension. The structural layer thickness of the accelerometer is 4μm. First, the accelerometer design is described, followed by an overview of the fabrication and characterization process. The released devices have been electro-statically analyzed, with an impedance analyzing system, in order to verify the DC responses of the devices to bias voltage sweeps. Then, the devices are encapsulated in a DIL (Dual-in Line) package for the vibration and angular characterizations. The dynamic responses of the poly-SiGe devices are compared to those of a piezoelectric reference accelerometer. The results demonstrate for the first time the achievability of fabricating large sensing area, low g accelerometers with the above-CMOS poly-SiGe technology.

Keywords: Capacitive accelerometer; SiGe; Low thermal budget MEMS; MEMS above-IC

1. Introduction

MEMS accelerometers have been widely used in many sectors of industry and consumer electronics. Techniques such as bulk and surface micromachining have substantially improved the performance of accelerometers over the years [1]. Meanwhile, monolithic integrated accelerometer research has become a promising research field, by means of which the monolithic integration of a micro-sensor and the related interfacing integrated circuit can be realized. Among the monolithic integration technologies, MEMS above-IC integration benefits from the use of standard CMOS, miniaturized size and possibly low cost [2-4]. On the other hand, among all the detection principles, the capacitive accelerometers feature high sensitivity, stable DC-characteristics, low drift, low power dissipation and low temperature sensitivity [5]. Therefore, to realize capacitive accelerometers by above-IC integration shows great promise. The major restriction for a post-CMOS integration technology is to find the proper

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material with a low processing thermal budget. Poly-SiGe turns out to be a promising choice since it possesses similar mechanical properties as poly-silicon and can be deposited on top of CMOS due to its low processing temperature (~450 ºC) [6].

This paper presents a low g capacitive accelerometer fabricated in a 4 µm thick poly-SiGe structural layer. Figure 1 shows the proposed parallel-plate shaped device. The device features an effective capacitive surface of 2.55×10^5 μm^2, suspended by four folded beams of 500µm effective length. The devices demonstrated here are intended to prove the ability to fabricate reliable accelerometers in the SiGe process, before actually merging the process in the envisaged above-CMOS process. To test the devices, an impedance analyzer is used first to check the electrostatic response of the device to a DC bias voltage sweep across its counter electrodes. Thereafter, the device is wire bonded to a MS3110 capacitive readout integrated circuit and encapsulated in a DIL (Dual-in Line) package for the dynamic and angular characterization.

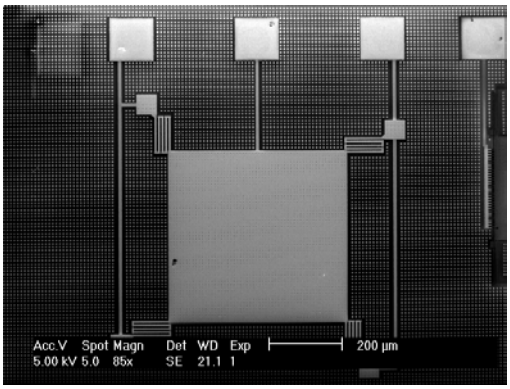

Fig. 1: Realized poly-SiGe low-g capacitive accelerometer (SEM top view)

2. Device fabrication

Figure 2 illustrates the fabrication process flow of the poly-SiGe low-g capacitive accelerometer. The fabrication process starts from a silicon wafer with a silicon oxide layer to mimic the CMOS backend and a SiC passivation layer. The SiC layer is used to protect the oxide layer from the HF release step later on. On the SiC layer, the SiGe electrode layer is deposited by CVD (Chemical Vapor Deposition) and patterned, Figure 2 (1). Then the sacrificial oxide layer is deposited and patterned, Figure 2 (2). Openings are made to place the anchors. The following step is to deposit the structural SiGe layer. A 4µm thick structural layer is realized by CVD seed layers and PECVD (Plasma Enhanced CVD) consecutive deposition of four 1µm layers, with chamber cleaning steps between subsequent layers, Figure 2 (3). An additional oxide deposition is conducted for the metal bondpad via, Figure 2 (4). The bondpad layer is then deposited on top and patterned, Figure 2 (5). The SiGe structural layer is then patterned, masked by the oxide layer on top, Figure 2 (6). The last step is to release the whole stack with HF, Figure 2 (7).

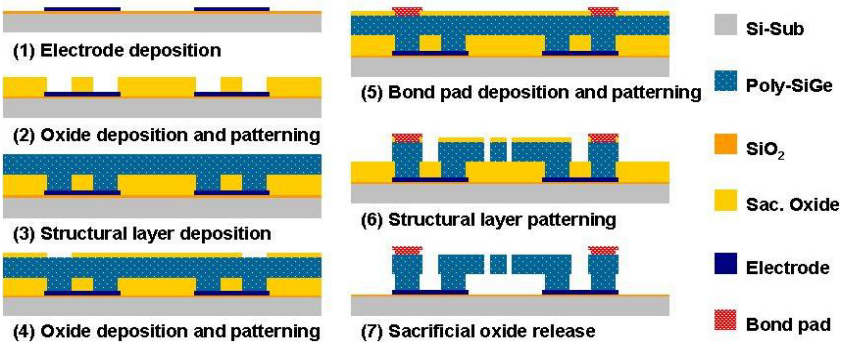

Fig. 2: Fabrication process flow of the poly-SiGe low-g capacitive accelerometer

3. Device characteristics and discussion

The fabricated devices are characterized electrostatically first, using a DC voltage sweep with a HP4194A impedance/gain-phase analyzer. After this functional test, the Device Under Test (DUT) is then bonded to the interfacing capacitive readout chip and encapsulated in a DIL package for the vibration test (Figure3).

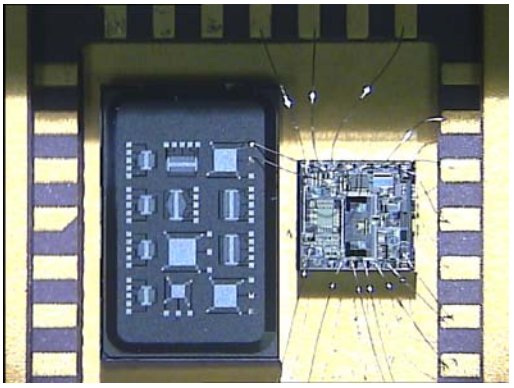

Fig. 3: DUT being bonded to the interfacing capacitive readout chip encapsulated in a DIL package

The dynamic tests are performed on a vibration test setup, consisting of a shaker, a piezoelectric reference accelerometer and a data acquisition system. Three major sets of tests have been conducted, including sinusoidal actuation tests at different frequencies (ranging from 3Hz to 1 kHz), periodical shock tests and random shock tests. Both the time domain (Figure 4) and the frequency domain (Figure 5) responses have been acquired, allowing a comparison between the DUT and the reference accelerometer. Similar results have been acquired across the actuation frequency band. The test results show that the DUT performs comparable with the VTI G012BA commercial reference accelerometer.

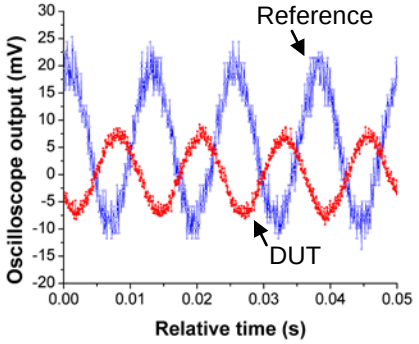

Fig. 4: Time domain responses of the DUT and the reference accelerometer with 80Hz sinusoidal actuation

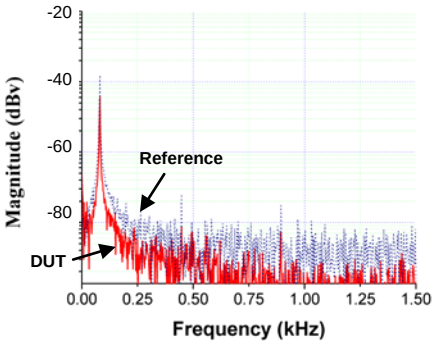

Fig. 5: Frequency domain responses of the DUT and the reference accelerometer with 80Hz sinusoidal actuation

The angular test has been implemented by using a rotational holder (Figure 6), to determine the response of the DUT to the projected portion of the gravitation to its main axis (Figure 7). The test results demonstrate that a low-g accelerometers with large capacitive sensing surface can be achieved with this optimized poly-SiGe surface MEMS technology. The fabricated device can sense the gravitation projection to the main sensing axis with the average sensitivity of 0.5 mV/°.

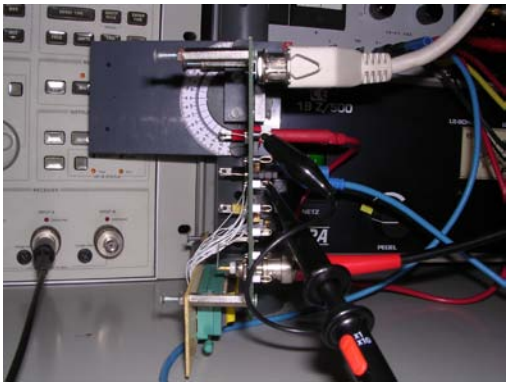

Fig. 6: Close view of the Angular test setup (with ASIC configuration cable and monitoring probes)

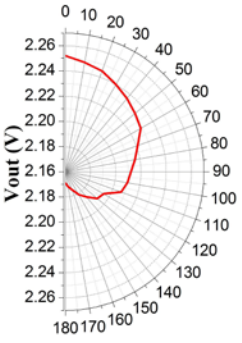

Fig. 7: Polar diagram of the DUT's Angular response, when Cf=0.513pF (Cf, the feedback capacitor of the charge amplifier on the ASIC)

4. Conclusion

This paper clearly demonstrated the adoption of the low temperature SiGe process to yield functional inertial sensors. A low-g capacitive accelerometer has been designed and fabricated above a silicon substrate with passivation layer. The released devices have been electrostatically analyzed before encapsulated in a Dual-in Line package for the vibration and angular characterizations. The vibration test results have been compared between the DUT and the VTI G012BA reference accelerometer. The comparisons show that the performance of the SiGe accelerometer is comparable with the commercial counterpart. The angular test demonstrates that the DUT is capable to sense the gravitation projection to the main sensing axis with the average sensitivity of 0.5 mV/°.

Acknowledgements

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